REMARKS

The Official Action dated April 5, 2007 has been received and its contents carefully noted. In view thereof claims 1, 21 and 26 have been amended in order to better define that which Applicant regards as the invention. As previously, claims 1-29 are presently pending in the instant application with claims 6-20 being withdrawn from further consideration by the Examiner as being directed to a non-elected invention.

With reference to the Official Action and particularly page 2 thereof, Applicant again confirms the election of claims 1-5 and 21-29 for prosecution on the merits, this election being made without traverse on February 11, 2005.

Further on page 2 of the Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of U.S. Patent No. 5,177,745 issued to Rozman, U.S. Patent No. 6,112,322 issued to McGibney et al. and U.S. Patent No. 6,037,792 issued to McClure. This rejection is respectfully traversed in that the combination proposed by the Examiner, now including the teachings of Rozmen, neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

In this regard, as can be seen from the foregoing amendments to independent claim 1 as well as similar amendments carried out with respect to independent claims 21 and 26, Applicant's claimed invention now recites a nonvolatile semiconductor memory device comprising a memory cell array having a plurality of memory cells and arranged in an array, the cells being connected to a plurality of bit lines and word lines, a plurality of address input terminals inputting a plurality of addresses thereto, a test mode circuit for outputting a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality address input terminals when a signal is inputted to the predetermined terminal among the

address input terminals, a row decoder connected to the test mode circuit with the test mode signal being inputted to the row decoder for applying an excess voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state in response to the test mode signal and a monitor terminal connected to the test mode circuit and outputting the test mode signal for confirming a test mode. That is, in accordance with the present invention, the nonvolatile semiconductor memory device includes a test mode circuit which inputs a test mode signal to the row decoder and a monitor terminal connected to the test mode circuit for outputting said test mode signal for confirming a test mode.

In rejecting Applicant's claimed invention, the Examiner states that Applicant's Admission includes a test mode circuit for outputting a test mode signal according to a predetermined voltage being supplied to a predetermined terminal when a signal is inputted to the predetermined terminal. The Examiner states that it is implied from the Admissions that the test mode circuit is provided for controlling the operations of columns. Further, the Examiner is of the position that a signal from the exterior implies that the test mode circuit for outputting the test mode signal according to a predetermined voltage being supplied to a predetermined terminal when the signal is inputted to the predetermined terminal is likewise shown by Applicant's Admissions, however, it is respectfully submitted that Applicant's Admissions do not show that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal of a plurality of address input terminals. Additionally, it is respectfully submitted that Applicant's Admitted Prior Art fails to disclose or suggest providing a monitor terminal for confirming a test mode of the memory device from the outside. Further, and more importantly, Applicant's Admissions fail to disclose or suggest that the test mode signal is inputted to the row decoder for applying an excess voltage

for a test to all word lines. Thus, it is respectfully submitted that Applicant's Admitted Prior Art is significantly different from that of the present invention. Moreover, it is respectfully submitted that neither the teachings of Rozman, McGibney et al. or McClure et al. overcome such shortcomings.

The Examiner appreciates and states that Applicant's Admission does not teach that the predetermined terminal is that among or of the plurality of address input terminals; and a monitor terminal (or pad) connected to said test mode circuit and outputting said test mode signal for confirming a test mode. The Examiner further appreciates that Applicant's Admission fails to disclose that the row decoder is connected to said test mode circuit and applies said excess voltage to all said word lines. In view of these shortcomings, the Examiner now relies on the teachings of Rozman as well as those references previously relied upon. It is noted; however, that Rozman merely discloses a test mode detection and trigger circuit 28 for detecting a test mode according to a voltage of a predetermined address pin. Rozman clearly fails to disclose or suggest that the monitor terminal and that the test mode signal is inputted to the row decoder for applying an excess voltage for a test to all word lines as is specifically recited by Applicant's claimed invention. Consequently, the combination proposed by the Examiner, including the teachings of Rozman, fails to render obvious that which is presently set forth by Applicant's claimed invention.

As noted previously, McClure et al. merely discloses that the burn-in test mode circuit 10 is controlled by ETD pulse which is triggered by a change in state of an address pin. However, McClure et al. clearly fails to disclose or suggest that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal of a plurality of address input terminals. Further, it is noted that McClure et al. discloses a device pin 48 and test flag 54; however, the signal outputted to the device pin 48 or test flag 54 is a

ground voltage supplied by a transistor 50 or an output signal of an inverter 52 in that the pin 48 and flag 54 do not receive the test mode signal directly. Clearly, McClure fails to disclose or suggest that the test mode signal is inputted to the row decoder for applying an excess voltage for a test to all word lines. Still further, McClure is not capable of confirming that the excess voltage has been applied to all word lines indirectly by monitoring the voltage of the test mode signal on a monitor terminal as with the present invention. Consequently, this reference likewise fails to disclose that which is presently set forth by Applicant's claimed invention.

As to the teachings of McGibney et al., this reference merely shows a control circuit CTRL receiving an initiation signal GO to control a stress test for selecting two word lines sequentially. Further, McGibney et al. fails to disclose or suggest a monitor terminal for confirming the test mode of the memory device from the outside. McGibney et al. does not disclose a monitor terminal for outputting the signal 404 and the signal 404 is not inputted to the decoder 402. Thus, the signal 404 does not correspond to the test mode signal of the present invention. Accordingly, it is respectfully submitted that McGibney et al. likewise fails to overcome the shortcomings associated with Applicant's Admissions as applied by the Examiner.

Therefore, in that the references relied on by the Examiner as well as Applicant's Admissions, clearly fail to disclose or suggest that which is presently set forth by Applicant's claimed invention, it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 as well as those claims which depend therefrom clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

Turning now to page 5 of the Office Action, claims 2, 22 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admissions in view of Bozman, McGibney and McClure as applied to claims 1, 21 and 26 and further in view of teachings of U.S. Patent No. 5,982,677 issued to Fontana et al. This rejection is likewise respectfully traversed in that the patent to Fontana et al. fails to overcome the aforementioned shortcomings associated with the combination proposed by the Examiner.

As noted previously, Fontana et al. merely discloses a structure of a regulator. More particularly, Fontana et al. fails to disclose or suggest a monitor terminal for outputting the test mode signal, nor does this reference disclose or suggest tha the test mode signal is inputted to the row decoder for applying the excess voltage for the test to all word lines. Consequently, it is respectfully submitted that while Fontana et al. may disclose the drain voltage regulator referred to by the Examiner, this teaching clearly fails to overcome the aforementioned shortcomings associated with the combination proposed by the Examiner. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 as well as claims 2, 22 and 27 which depend therefrom clearly distinguish over the combination proposed by the Examiner and is in proper condition for allowance.

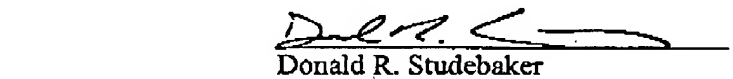
With reference to the Examiner's response to Applicant's arguments, set forth in paragraph 7 of the Office Action, it is respectfully submitted that in accordance with the teachings of McGibney the signal 404 is not inputted to the decoder 402. Thus, the signal 404 does not correspond to the test mode signal of the present invention in that McGibney et al. fails to disclose or suggest providing a row decoder connected to said test mode circuit with the test mode signal being inputted to the row decoder for applying an excess voltage for a test to all said word lines in response to said test mode signal. Consequently, it is respectfully

submitted that Applicant's claimed invention clearly distinguishes over the combinations proposed by the Examiner and is in proper condition for allowance for at least the reasons discussed hereinabove.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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